Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO.	SERIAL NO.
		242006US2	NEW APPLICATION
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Toshifumi IWASAKI	
		FILING DATE	GROUP
		HEREWITH	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
CVL	AO	11-186495	07/09/99	Japan (with English extract)		x
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

CVL	AW	Gregory SCOTT, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", IEDM, IEEE, 1999, pgs. 827-830
	AX	
	AY	
	AZ	

☐ Additional References sheet(s) attached

Examiner [signature] Date Considered 8/4/06

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.